Homework 2

(Due date: October 7th @ 7:30 pm)

Presentation and clarity are very important! Show your procedure!

Problem 1 (20 pts)

- Convert the following signed fixed point numbers in format [16 8] to the dual fixed point format 16_8_3. If more bits are required, you are allowed to use the format 17_8_3.

FX	FA.09	09.3E	09.FA	8A.91	80.AE	81.E4	8A.12	AB.CE
DFX								

Problem 2 (30 pts)

- Calculate the result of the following operations where the numbers are represented in dual fixed-point arithmetic. Note that the results must be in the same format. Include an overflow bit when necessary.

DFX Format: 8_4_2	Result	overflow		Result	overflow
FA+09			EB+A3		
FB-90			C0+C2		
43+7A			F6+34		

DFX Format 16_8_4	Result	overflow		Result	overflow
FA2A+0A09			F939-0932		
C000+F1C3			F343-6A99		
FFF0-081B			BEEF-FADE		

Problem 3 (50)

- Design the following signed multiplier circuit ($N = 12, M = 8$). Use the structural description in VHDL. Create a different VHDL file for each circuit (FSM, registers, adder/subtractors).
- Create a testbench to test the following cases. Complete the table.

A	FED	48A	78C	78D
B	FC	FE	F4	61
P				

- Attach a printout of your VHDL and testbench files.